Optimizing Enterprise-Class SSD Host Controller Design with Arteris FlexNoC Network-On-Chip Interconnect IP

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Abstract—As solid-state disk technology replaces hard disk-drive technology in enterprise data centers, designers of SSD controller chips are tasked with introducing highly complex designs during a period of rapid market transition. Traditional interconnect technology such as busses, crossbars, grids or hybrid solutions used in hard-disk drive controllers has not kept pace with the growing complexity that SSD controllers require. The use of advanced network-on-chip intellectual property can replace traditional interconnect solutions to significantly improve the manageability of designing SSD controllers and enhance devices in terms of performance, latency, reliability, power consumption, cost and time-to-market.

Keywords—SSD reliability; SSD controller; SSD host controller; solid-state drive; enterprise storage; data center storage; SoC interconnect; on-chip interconnect; SoC; system-on-chip; NVMe; network-on-chip; Arteris FlexNoC; bus; crossbar.

I. Introduction

Hyperscale data centers, especially those running virtualized environments requiring the lowest latency and highest performance, are undergoing a massive technology shift in the way information is stored, accessed and processed. Older hard-disk drive (HDD) technology is being replaced on a large scale by solid-state drive (SSD) technology because it is faster, more scalable and consumes less power, which leads to lower cost. [1]

As a result of this massive transition from rotary to solid state storage, many technology providers are jumping on board to deliver the highest performance solutions in order to achieve market differentiation. One specific area that is a focal point of this transition is the SSD host controller. [2] Integrated circuit designers here are in a competition between incumbent consumer SSD and HDD designers and emerging players. Both are trying to deliver the highest performance, the greatest data protection, the lowest latency, and best power efficiency with the most advanced features.

Delivering the right combination of features and performance is difficult because enterprise SSD controllers are some of the most complex system-on-chip (SoC) devices ever designed. However, a few of the competitors are differentiating their designs through a network-on-chip interconnect intellectual property
known as Arteris FlexNoC. Through this on-chip fabric, designers are able to create chips that are higher in performance, better at data protection, and lower in power consumption than those ICs with interconnects designed using conventional methods. Additionally, FlexNoC interconnect fabric IP improves the manageability of the project and enables chip design teams to overcome many of the difficulties that have historically delayed complex SoC design schedules and caused them to miss market introduction schedules.

By further examining the emerging performance parameters that enterprise SSD controllers need to deliver and by exploring the role that FlexNoC Interconnect IP plays in enhancing performance and enabling better management of the design process, chip designers will learn a better strategy to deliver SoCs that are superior to the competition in a timeframe that provides a market advantage.

II. ENTERPRISE SSD HOST CONTROLLER TECHNOLOGY

A. SSD Technology Advantages Versus Electromechanical Disk Drives

As technology evolves, key performance parameters of SSD technology have advanced to the point where performance, bandwidth, reliability, cost and latency factors provide superior alternative to 15,000 RPM HDD technology in hyperscale data centers [3]. Compared with electromechanical disks, SSDs are typically more resistant to physical shock, run silently with less energy loss, have lower access time, and less latency. [4] Enterprise flash drives (EFDs) are designed for applications requiring high I/O performance (IOPS), reliability, energy efficiency and, more recently, consistent performance. In most cases, an EFD is an SSD with a higher set of specifications, compared with SSDs that would typically be used in notebook computers. [5]

B. Unique Requirements for Enterprise SSD Host Controllers

One of the primary keys of SSD performance is the host controller. Every SSD includes a controller that incorporates the electronics that bridge the NAND memory components to the host computer. [6] The host controller chip serves as the “mother” controller, which in turn communicates with multiple “daughter” controller chips attached to specific banks of flash memory. The controller is an embedded processor that executes firmware-level code and is one of the most important factors of SSD performance. [7]

Unlike current consumer class SSD controllers that max out at 1 or 2 terabytes (TB), current enterprise class devices need to access to 10 TB of data storage and demonstrate a roadmap of scalability that enables data center managers to plan a roadmap 10 years into the future. [8]

Enterprise-class controller chips need to be scalable, to allow end-users to cascade multiple SSD “slices” as dynamic storage needs change. [9] Today’s controllers make it possible for SSDs to deliver 310,000 I/O operations per second (IOPS) for mixed read/write workloads. These workloads are typical of those required
by a variety of performance critical data center applications, such as traditional and scale-out databases, virtualization, and big data analytics. [10]

Leading performance features [11] of enterprise class SSD host controllers are:

- **Ultra-low latency:**
  - Especially for communications to and from ARM Cortex-R5 or R7 low latency peripheral ports;
  - NVMe, short for Non-Volatile Memory Express, is an emerging standard providing lower latency. This is mostly due to a streamlined storage stack and the fact that NVMe requires no register reads to issue a command. NVMe is superior to AHCI, which requires four uncachable register reads per command, resulting in ~2.5µs of additional latency.

- **Extremely high bandwidth:**
  - 4K page size restrictions per transaction on ARM AMBA architecture have a limiting factor on performance but enterprise-class SSDs require large block transfers in a scheme known as Logical Block Addressing (LBA);
  - Cascading slice approach enables enterprise-class devices to access up to 10TB of storage.

- **Low Power:**
  - A leading concern in data centers is power consumption both in terms of the average compute power and the cooling resources required to keep equipment operating at optimal performance levels;

- **Data Protection:**
  - Chip designs require more data bits for Error-Correction Coding which involves adding logic for ECC encode and decode and hardware duplication to equal and surpass the reliability of HDD technology.

Integrated circuit design teams have to integrate several key functional IP blocks in order to produce an advanced SSD controller. Getting a design off the drawing board and into volume production ranks as high in importance as performance for the makers of SSD drives.

Since SSD controllers are some of the most complex chips ever designed, teams must manage their projects carefully in order to integrate all the necessary performance, data protection and power consumption features that are required to meet the enterprise data center benchmarks.
The following block diagram demonstrates all of the features, blocks and subsystems that SoC design teams must consider:

![Block Diagram](image)

**Fig. 1. Enterprise SSD Controller High-Level Design**

### III. ROLE OF THE ON-CHIP INTERCONNECT

There are many more independent engines on an enterprise SSD controller than other chips of comparable complexity, such as consumer-class SSD controllers or even mobile phone application processors. During the design process, the connections between these engines can overwhelm the layout team with an unmanageable amount of metal lines. On-chip interconnect efforts conducted via traditional industry topologies, such as, bus, crossbar, fabric or hybrid types, are inefficient at accommodating this physical complexity. This can result in design problems that occur in place and route. Problems such as routing congestion and the resulting timing closure delays can push out design schedules dramatically, eat into margins, and even drive project costs to unsustainable levels.

Since the interconnect links all the individual subsystems on the chip, and since it is the last IP to be configured, the engineers on the interconnect team usually assemble all the different pieces of the design. This also provides them with the opportunity to address a range of design-wide challenges in an expeditious manner. In complex SoC designs, for example, the use of network-on-chip (NoC) IP has been used to streamline debugging, reduce SoC complexity and pre-empt back-end routing challenges that teams typically face.
A. Commercial Network-on-Chip Technology: Arteris FlexNoC

Arteris FlexNoC is a network-on-chip IP that requires fewer wires than traditional interconnect methodologies. As a result, FlexNoC enables an easier place and route process for chip designs and allows designers to avoid some of the typical routing and congestion problems that push out design schedules. [12]

Additionally, the FlexNoC IP provides a proven vehicle to improve the performance, enhance data protection measures and cut power consumption of complex SoC designs. Unlike most IPs in hard macro form, FlexNoC’s synthesizable IP is designed to stretch across the die and remain elastic in shape, allowing it to be placed within the “white space” between other IPs. This capability enhances back-end timing closure tremendously. In addition, the FlexNoC Physical IP allows integration with the back-end tool flow through, for example, placement information like DEF and LEF, and insertion of pipeline stages for easy place and route implementation. FlexNoC Physical has been proven to significantly reduce back-end implementation time and effort.

An example of the implications of NoC interconnect configuration on semiconductor physical design are shown in Figures 2 and 3 on the following page, which show place and route congestion maps for a small chip layout with varying data link widths. Fig. 2 illustrates possible wire routing congestion using NoC RTL with zero header serialization cycles, meaning that packet header information is transmitted in parallel to data. Fig. 3 shows reduced wire congestion using NoC RTL with header serialization optimized so that width of each link is equal to the widths of the data on the link, meaning that header data is transmitted serially with the data over fewer wires.

![Place and route congestion map of NoC interconnect with zero header serialization cycles.](image)
Reducing link widths in the RTL in order to reduce the number of wires allows the downstream EDA tools to reduce peak congestion, shown in red. At the same time, having fewer wires for the same amount of IP logic allows congestion to be spread more widely, as seen in the lower blue and yellow regions.

IV. SOC PERFORMANCE AND ON-CHIP INTERCONNECTS

In a system-on-chip, the interconnect links processors and coherence controllers, last-level system caches, memory and on-chip peripherals. Increases in CPU performance are only realized with a corresponding increase in interconnect bandwidth. Thereby, the performance of the on-chip interconnect constrains overall SoC performance. There are many detailed considerations required for a low-latency interconnect in a high-performance CPU-based SSD host controller. [13]

FlexNoC enables a flexible data path design to optimize for low latency and high bandwidth. This concept is often called quality-of-service (QoS). End-to-end QoS enables individual paths can be optimized based on design requirements. For each path, NoC technology allows tradeoffs between the number of wires, performance and area. If required, designers can configure paths for zero latency between an initiator and a target to make the trade-off between wires and bandwidth on a per-link basis.

In comparison to traditional interconnects, NoC technology enables designers to:

○ Maximize system performance on performance critical paths, and minimize area and wire count on other paths

○ Simulate and explore multiple candidate architectures and topologies to ensure performance requirements are met.

○ Guarantee quality-of-service requirements for path latency and bandwidth.
In summary, flexible NoC interconnect IP enables per-path optimization in complex enterprise-class SSD controller designs. This enables designers to maximize system performance on critical paths and to minimize area and wire count on other paths.

V. ERROR RESILIENCE, ENDURANCE AND END-TO-END DATA PROTECTION

Due to data center SSD endurance and error resilience requirements, many SSD controller developers use the ARM Cortex-R5 and Cortex-R7 processors because they employ techniques such as ECC and parity data protection and other advanced features. However, this CPU-centric approach neglects to provide end-to-end protection from initiator to target throughout the rest of the SoC. End-to-end protection can only be provided by implementing resilience features in the on-chip interconnect.

A. Advanced Data Protection and Reliability for SoC Interconnects

Arteris FlexNoC expands data protection and reliability features beyond the CPU and into the network-on-chip interconnect fabric. [14] FlexNoC can pass IP-generated error-correcting code (ECC) information through the NoC between socket interfaces. Alternatively, FlexNoC can generate custom data payload and control ECC in packet-generating units, and detect or correct errors in packet-consuming units. The amount of redundancy per data byte is configurable based on the cost and resilience requirements of the SSD controller.

The FlexNoC Resilience package also includes packet validity checking, transaction timeout, control register parity checking and unit duplication and comparison that are all designed to extend error resiliency beyond the CPU and into the other hardware blocks of the design. Key to a complete implementation is the inclusion of a safety controller to manage faults and a fully-verified built-in test (BIST) module to continually test data protection hardware when activity is quiescent.
Additional FlexNoC data protection features help SSD developers offer end-to-end data protection down to the per-byte level:

- Core interface protection supports user-defined protection schemes;
- Core-side protection logic -
  - Detects and corrects errors upon transaction requests;
  - Generates protection semantics to IP core upon transaction responses;
- Packet transport protection logic detects and corrects transport-level errors.

VI. REDUCING POWER CONSUMPTION

Even relatively minor reductions in SSD power consumption can have a huge impact on data center power consumption. Designers have reduced power use by switching from a hybrid-bus interconnect architecture to an advanced NoC interconnect fabric. The following power advantages have been proven in the most complex designs that have achieved high-volume production by implementing Arteris FlexNoC: [15]

- Decrease active power consumption to 0.7 milliwatts over a 1-million gate block;
- Reduce die size by 5-10%;
- Drop idle leakage power by 7x;
- Cut the number of wires by 50 percent;
- Shrink gate count by 30-to-50 percent.

A. Advanced power management features

Similar to ECC, many SoC power saving measures have traditionally been implemented only in the CPU. NoC IP provides the ability to manage power consumption across all the functional blocks on the SoC and all the connections between them, not just in the CPU and GPU subsystems. Figure 5 below provides examples of how NoC clock, power and voltage domain portioning provides SoC. Data center operators are very conscious about the heat dissipation from server equipment, the amount of energy required to keep equipment running for optimal performance and the overall cooling requirements for data center equipment. Chips that are lower in power consumption than their peers have a market advantage in data centers.
Specific FlexNoC features to reduce power consumption of SSD controllers include:

- Dynamic Voltage Frequency Scaling (DVFS);
- Power gating of different power domains to control signals and ensure safe shutdown/wakeup;
- Gating off of different clock domains to control signals and safely cut off clock domains;
- Unit-level clock gating for idle units within the NoC;
- Local clock gating performed by synthesis tools;
- Isolation cells, level shifters, UPF.

VII. MAINTAINING SCHEDULE PREDICTABILITY

FlexNoC interconnect IP has been instrumental in helping SoC design managers to organize their global teams based on a hierarchy of design challenges by affording greater flexibility to respond to changing requirements. Compared to using obsolete, tiered bus or crossbar architectures for the SoC fabric, NoC technology is more effective in reducing the complexity of SoC designs. It also enables faster debugging and back-end placement and timing closure. Arteris FlexNoC has been proven to reduce the probability of a design project schedule slip, and improve the ability to introduce SoCs earlier than planned.

A. NoC composition for distributed design

One particular feature of FlexNoC, called NoC Composition, is useful for integrating all of the individual interconnects for all the SoC subsystems into one system view that can be comprehensively verified. FlexNoC Composition has enabled design teams to cut development time from 18 months to as little as nine months in the most complex SoCs. Composition enables project managers to parcel out the design tasks to
separate teams, whether they work in the same building or work in distributed design centers around the world. Furthermore, composition enables automated integration of subsystems coming from acquired companies.

Compared to hybrid buses or crossbars, NoC Composition allows all the interconnections between the separate blocks to come together seamlessly. By making the SoC easier to reassemble, the final verification process for the chip is much easier and faster. The end result is a shorter development time, shorter time to market, and greater potential for revenue and profit.

VIII. CONCLUSION

Enterprise SSD controller market growth is reaching an inflection point as hyperscale data centers adopt SSDs to replace older HDD technology. Teams are wrestling with design complexities and data center requirements that could push out their schedules and delay their entry into this dynamic, high-volume market.

Network-on-chip technology can replace traditional interconnect approaches in SSD host controller designs and ultimately make the design process more manageable. In particular, Arteris FlexNoC brings a proven record of manageability to this market segment after enabling design teams of even the most complex SoCs reduce their schedules from 18-to-24 months, down to 9-to-12 months. In fact, FlexNoC is the proven NoC technology providing additional value by enhancing performance, reducing power consumption, and improving end-to-end data protection for enterprise SSD controllers.

REFERENCES


Dee Lin joined Arteris as a Senior Solution Architect in 2014. Since joining, he has worked with Arteris customers on various applications from front-end to back-end implementation. With over 10 years of experience in the semiconductor industry, Dee has worked on wide range of system-on-chip projects such as application processors, microcontrollers, networking processors, automotive ICs, and solid-state drive controllers.

Prior to joining Arteris, Dee held engineering positions at OneSpin Solutions, Sonics, and National Instruments.

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Prior to Arteris, Kurt held senior marketing leadership and product management roles at Intel, Texas Instruments, ARC International and two startups, Virtio and Tenison. He has extensive IP, semiconductor and software experience in the mobile, consumer electronics and enterprise server markets. Before working in high technology, Kurt flew as an air commando and navigator / electronic warfare officer in the U.S. Air Force Special Operations Forces.

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