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**ARTERIS SHIPS ARTERIS NoC SOLUTION 1.4
TO ACCELERATE ADOPTION OF NETWORK ON CHIP**

New version of Arteris NoC IP library and design tools enhance productivity for constructing on-chip communications subsystems; Adds AMBA® 3 AXI support

PARIS, France – February 27, 2006 – Arteris SA, a leading provider of Network on Chip (NoC) solutions addressing challenges associated with on-chip communications, today announced immediate availability of its Arteris NoC Solution, Version 1.4. The latest release of the IP library and accompanying tool set incorporates a range of customer feedback and includes new productivity-oriented features and tighter integration with EDA tool flows that will accelerate the implementation of NoC-based methodologies in complex SoCs.

Arteris also announced support of the AMBA® 3 AXI™ protocol from ARM as part of this release.

Specific enhancements in the Arteris NoC 1.4 solution include:

- Improved automation in NoCexplorer™, the company's tool for evaluating NoC architecture and chip topologies;
- Improvements in how IP 'socket' standards are handled, including support for AMBA 3 AXI with a new network interface unit (NIU) for the Arteris solution;

- A new NoC Self-Test Generator™ which helps ensure that each NoC instance and its associated interface protocol meet architectural specifications;
- A new NoC Trace and Debug™ capability to verify performance and behavior characteristics during SoC simulation.

“The Arteris NoC Solution 1.4 is the third production release of the only commercially available Network on Chip SoC communications solution and one that incorporates not only major new features but significant user feedback as well,” said Charlie Janac, President and CEO of Arteris. “We are committed to enabling the transition to NoC-based chip design in order for customers to obtain lower SoC unit costs, manage system complexity and performance, and facilitate more efficient IP integration and reuse. This latest release enhances our ability to do that.”

Arteris broke new ground when it introduced the first commercially available NoC solution in 2005. The Arteris NoC is a three-layer packet switching network that operates inside complex SoCs. The solution uses an innovative IP library of switches, network interface units, and other soft IP blocks that allow Arteris customers to configure their own flexible SoC communication subsystems. The NoC technology improves upon traditional bus-based approaches that must be redesigned for each different type of SoC configuration, and typically use more wires, consume more power with lower performance, while often increasing die size.

The Arteris NoC Solution integrates easily with popular EDA design flows through RTL outputs in Verilog, VHDL and System C formats, together with synthesis scripts.

New productivity features in Arteris NoC Solution 1.4

The NoCexplorer 1.4 tool dramatically increases the automation required to integrate IP blocks with an NoC. The intuitive and graphically-oriented tool enables system architects to quickly evaluate the impact of fundamental architectural alternatives to design a NoC topology that meets their SoC specifications – at the earliest stages of the design cycle. Even with modest amount of data, SoC traffic parameters such as operating

frequency, latency, bandwidth, and quality of service can be quickly and accurately analyzed. NoCexplorer 1.4 provides an analysis of the impact of sharing hardware resources for multiple dataflows. The output of this NoC exploration phase is the application-specific topology of the Arteris NoC instance compatible with the specified SoC communication constraints. The company's NoCcompiler™ tool then customizes and connects the Arteris NoC Library IPs to generate an RTL version of the NoC instance, which can then feed into existing EDA flows.

The Arteris solution enables faster and easier IP reuse by decoupling the SoC communication protocol from the IP socket standards, delivering a productive design methodology and enhanced IP use flexibility. Arteris is capable of supporting multiple IP communications protocols, a capability enhanced with the delivery of the new AXI protocol NIU in addition to existing support for AMBA and proprietary format NIUs.

The latest release of the Arteris solution also addresses IP quality issues. The new Arteris NoC SelfTest Generator allows users to test that each generated Arteris NoC instance, with its associated IP protocols, complies with its original specification - including its specified behavior down to its components including sockets, address map and connection map before it is integrated in the SoC. The NoC SelfTest Generator is able to check assertions and report performance properties such as end-to-end, latency and peak throughput for any Arteris NoC instance configuration.

SoC-level performance verification consumes an increasing portion of SoC development time. The new NoC Trace and Debug tools in the Arteris solution allow verification that SoC communication performance objectives have been met once the NoC has been configured and inserted in the SoC. Inserting a trace mechanism in the Arteris NoC instance allows measurement of NoC performance results such as bandwidths and latencies, and debugging of transaction and link-level performance during simulation.

“Designers are looking to NoC in general, and Arteris specifically, for a host of benefits this approach brings for on-chip communication and IP integration and re-use – fewer global wires, higher performance, lower power and smaller die size. With this latest release we offer even more capabilities take advantage of the NoC concept and improve overall designer productivity,” said Pierre Huon, vice president of engineering at

Arteris. “The release of an Arteris Network Interface Unit for the popular 3AXI protocol further strengthens the ability of Arteris to support market leading IP blocks without modification and enable more efficient IP reuse.”

Pricing

The Arteris NoC Solution 1.4 is available on either per project time based license or royalty pricing models.

About Arteris

Arteris, SA, provides Network on Chip solutions to transport and manage the on-chip communications within complex System-on-Chip (SoC) integrated circuits, increasing performance, reducing number of global wires, with lower power utilization while enabling the most complex, IP-laden designs. It allows chip developers to implement efficient and high-performance Network-on-Chip (NoC) designs, overcoming limitations of traditional layered or pipelined bus-based architectures. Arteris’ technology is scaleable in terms of the number of IP blocks designers can network, as well as with deep submicron silicon manufacturing processes. The NoC solutions are compatible with existing design flows and with IP interface standards.

The Paris-based company operates globally with offices in Boston and San Jose, California. Arteris has raised more than \$12 million in equity investment from an international set of venture capitalists, including Crescendo Ventures, Techno Venture Management and Ventech. More information can be found at www.arteris.com.

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