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Arteris unveils strategy, technology for enabling Network-on-Chip (NoC) design

The Network-on-Chip™ company to debut technology that scales with the needs of complex SoCs, addresses limitations of current on-chip interconnect approaches

PARIS, France—March 1, 2004. Arteris SA, a start-up based in Paris, France focused on developing network-on-chip (NoC) technology, today announced its strategy for addressing the increasingly challenging requirement to create and manage data networks on complex integrated circuits (ICs), or system-on-chips (SoC). The company, founded by several semiconductor industry veterans, plans to introduce a unique and patented approach to enable chip designers and system architects to effectively build the communications 'networks' for chips comprised of many discrete building blocks. The approach promises to further the potential of design reuse and more effectively enable 'plus-and-play' semiconductor intellectual property (IP) use.

Arteris plans to introduce its first products, which will be a combination of EDA-style tools and licenseable IP components, in the second half of 2004. The company will also announce partnership programs with key EDA, IP and foundry partners in the next several months.

Arteris' innovation is based on a patented revolutionary switch fabric approach to transporting and managing the on-chip communication between individual SoC sub-systems, as well as across the entire SoC, an approach that is similar in concept to how computer networks are designed, implemented and managed. The technology, which scales and becomes increasingly critical with new process generations, enables a significant advancement over current layered or pipelined bus based interconnect strategies because it looks at the SoC network in its entirety, both in terms of architecture as well as on-chip traffic transport management. The Arteris technology is compatible with existing interconnect technology and IP interfaces, allowing designers to maintain their investment in those approaches and facilitating more efficient design reuse.

“Current methods of dealing with interconnect on SoCs, such as layered or pipelined bus based architectures, simply will not scale with the complexity and integration requirements of next-generation designs,” said Alain Fanet, president and CEO of Arteris. “Our technology addresses the entire on-chip communication challenge, not just individual interconnect. In that way, engineers can effectively build more efficient and higher performing designs. We do that in a way that provides an easier way to perform design reuse without a lot of custom interface work and is compatible with and preserves the investment made in earlier generation IP interface techniques.”

On-chip interconnect today is typically handled locally by a synchronous shared bus architecture, usually specific to the core being used. However, this method results in slower signal propagation as the size and complexity of the SoC increases, particularly as more IP blocks are added. Adding multiple buses introduces timing problems and general performance degradation to the design.

Arteris’ chip-wide—or global—approach uses a scalable switching fabric that is not limited by design size or number of cores. Using multi-purpose packets and narrower high-speed links, the technology allows higher wire efficiency than multi-layer bus approaches. This yields reduced die sizes and costs. It relies on a globally asynchronous, locally synchronous (GALS) approach that will become increasingly critical over time as wire delays to move a signal across the die approach one or several clock cycles, making timing closure of a fully synchronous approach difficult. The result is a single NoC architecture that allows faster timing closure by designers, facilitates plug-and-play design reuse, and scales with new generations of process technology.

Arteris’ solution is fully parametrizable, adapting to a wide variety of applications and topologies. The company’s solution is designed as an open, flexible architecture and supports any commercial or custom-made IP interfaces without changing system architecture each time a new CPU or IP library is used in the SoC design. Arteris’ technology also works seamlessly within existing EDA tool flows, and it enhances the process of floor planning and speeds timing closure. The ability to reach timing closure at a global level is especially important to SoC designers who currently struggle with fully synchronous approaches in complex, highly integrated chips.

Seasoned management team

Arteris’ three founders have long track records in the semiconductor industry, with an emphasis on telecommunications and network processor expertise. They are part of a group that founded T.Square, a network processor company that was eventually acquired by ADSL chip supplier Globespan, where the trio worked for several years together. Additional senior management adds design methodology, IP and design services experience.

Alain Fanet is Arteris’ CEO and in addition to his role as founder and president of T.Square also held senior management positions within Globespan and French semiconductor concern TEMIC. Cesar Douady is a co-founder and CTO of the company. His track record includes heading the development team of an increasingly complex DSL network processor line for T.Square, culminating in a 16-million transistor chip. Philippe Boucard is a co-founder and Chief Architect. He also worked at T.Square on DSL network processor design. Previously, he developed new communication concepts for network processor SoC interconnect.

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Kent Jaeger is Vice President of Marketing and Sales at Arteris. He has more than 20 years of marketing and sales management experience, including an extensive IP and design services background with EDA leader Cadence Design Systems, Inc., and its design services arm, Tality, as well as management roles at semiconductor companies Texas Instruments and AMD. Philippe Martin, is Vice President of Product Planning. He was formerly the Technical Director for Sonics Europe and has held senior management and technical positions at Mentor Graphics.

Arteris has raised more than \$12 million in early funding from an international set of venture capitalists, including Atlas Ventures, Crescendo Ventures, Techno Venture Management and Ventech.

About Arteris

Arteris, SA, develops technology to transport and manage the on-chip communication for complex integrated circuits and system-on-chips (SoC), an increasing concern in high performance, IP-laden designs. It allows chip developers to implement efficient and high-performance network-on-chip (NoC) designs, overcoming limitations of traditional interconnect approaches such as layered or pipelined bus-based architectures. Its technology is scaleable in terms of the number of IP blocks designers can network, as well as with silicon manufacturing process evolution. Arteris' technology works within existing design flows and with IP interface standards. The company, founded by semiconductor industry veterans and backed by an international set of venture capitalists, is based in Paris. More information can be found at www.arteris.net.

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