



For Immediate Release

For more information, contact:

Charlie Janac
Arteris, SA
+33 1 61 37 38 75
Charlie.janac@arteris.com

Mike Sottak
Wired Island, Ltd.
+1 408-876-4418
mike@wiredislandpr.com

ARTERIS STRENGTHENS TECHNICAL ORGANIZATION IN THE U.S.

Veteran Tool Development and Application Executives Join Arteris to Accelerate Delivery of Network on Chip (NoC) Products

PARIS, France – June 21, 2006 – Arteris SA, the leader in Network on Chip (NoC) Solutions for Complex System-on-Chips (SoCs), continued its global expansion with the addition of two key technical executives chartered with enhancing the ease and efficiency of adopting the company's innovative NoC offering. Joining Arteris in its San Jose, California office are Mr. Nafees Qureshy as Vice President, NoC EDA Development and Mr. Enno Wein as Director of Solution Architects. Both executives bring a broad breadth of experience in design tool and SoC development that will be instrumental in furthering the market penetration of Arteris' solution.

Qureshy will be responsible for leading the development of Arteris' design automation tool suite, which is critical for the implementation of NoCs used in complex SoCs for multimedia, telecom and wireless applications. The design solution, which consists of NoCexplorer™ and NoCcompiler™, is used to analyze and configure NoC options based on Arteris' proprietary intellectual property (IP). The Arteris NoC Solution™ integrates easily with popular EDA design flows through RTL outputs in Verilog, VHDL and System C formats, together with synthesis scripts. Qureshy was formerly the Vice President of Engineering at Jasper Design Automation and Senior Director of Engineering at CoWare where he was responsible for development of the ConvergenSC™ product line. He has also held engineering positions at Ikos System and Schlumberger. An experienced manager of distributed development teams, he will lead an Arteris NoC EDA software team that is based in both Silicon Valley and Paris, France.

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As Director of Solution Architects, Wein will manage application support for Arteris' NoC solution in North America, drawing upon his extensive background in chip design methodologies and physical implementation. His team will assist customers in the most effective use of the NoC concept, and work with them to develop design strategies that maximize the performance, area and IP integration benefits NoC offers. He was formerly the Chief Technical Officer of Element CXI and Monterey Design Automation and brings more than 20 years of complex SoC design experience to Arteris. At Element CXI, Wein headed a group that designed an internal NoC communication subsystem. He has also worked at Infineon and LSI Logic.

“The hiring of Nafees and Enno reinforces Arteris commitment to have both engineering and support resources close to North American customers and strengthens our overall technical team, both from a development as well as implementation perspective,” said Charlie Janac, Chief Executive Officer of Arteris. “Their experience in tool development, methodology optimization and IC implementation will be invaluable to customers transitioning to this important and necessary new design approach.”

Qureshy has an M.S., Computer Science from Arizona State University and Bachelor in Technology, Electrical Engineering from Indian Institute of Technology, Bombay, India. He will report to Pierre Huon, Arteris Vice President of Engineering.

Wein has an M.S., Electrical Engineering, from Technical University Carolo-Wilhelmina, Braunschweig, Germany and will report to Arklin Kee, Arteris Vice President of Business Development.

About Arteris

Arteris, SA, provides Network on Chip solutions to transport and manage the on-chip communications within complex System-on-Chip (SoC) integrated circuits, increasing performance, reducing number of global wires, with lower power utilization while enabling the most complex, IP-laden designs. It allows chip developers to implement efficient and high-performance Network-on-Chip (NoC) designs, overcoming limitations of traditional layered or pipelined bus-based architectures. Arteris' technology is scaleable in terms of the number of IP blocks designers can network, as well as with deep submicron silicon manufacturing processes. The NoC solutions are compatible with existing design flows and with IP interface standards.

The Paris-based company operates globally with offices in Boston and San Jose, California. Arteris has raised more than \$12 million in equity investment from an international set of venture capitalists, including Crescendo Ventures, Techno Venture Management and Ventech. More information can be found at www.arteris.com.

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