



Arteris and CoWare Announce Integration of Arteris Network on Chip (NoC) Technology into CoWare Platform Architect ESL Design Environment

ESL leader collaborates with NoC pioneer to provide full SystemC TLM models to facilitate leading-edge, on-chip communication solution

Paris, France and San Jose, CA – July 17, 2006 – Arteris, the technology leader for Network-on-Chip (NoC) technology and solutions, and CoWare[®], Inc, the leading supplier of platform-driven electronic system-level (ESL) design software and services, announced a comprehensive agreement under which Arteris will output SystemC transaction level models (TLM) from its NoC tool suite for incorporation into TLM platforms developed in CoWare Platform Architect.

As part of the collaboration, the companies will develop IEEE 1666 SystemC-based versions of the Arteris NoC building blocks that are compatible with CoWare's Platform Architect environment. Designers can utilize the Arteris tool suite to create RTL of the NoC, complete with synthesis scripts and test bench models, and then profile, debug and simulate both SoC hardware and embedded software implementations before silicon implementation. The Arteris tool set enables near real-time interaction and is driven by a familiar "spreadsheet" style of design.

"On-chip communications decisions are best made during the system-level design stage and this is an area where CoWare is a proven leader," said Charlie Janac, president and CEO of Arteris. "By incorporating the ability to design and analyze a NoC approach at this point in the design cycle, we are enhancing the designer's ability to maximize performance and integration benefits of SoC design in general and network-on-chip in particular. With the powerful combination of CoWare ESL design and advanced Arteris NoC technology, we will help lower both unit costs and project costs of complex SoCs for multi-media, telecom, and wireless applications."

The Arteris NoC methodology offers significant benefits to SoC designers who are developing complex chips using multiple IP and multiple processors, and are driving performance beyond 200 Mhz. For those chips, traditional bus-based architectures are fraught with timing closure, power consumption, and area problems that get increasingly difficult if not impossible to solve as process geometries dip to 90nm and below. At such density levels, gates are faster than wires and the Arteris NoC solution addresses the inherent challenges in bus-based designs. By integrating the Arteris technology with CoWare's ESL design tools, developers of complex SoCs have a complete solution for high-level design and NoC integration.

"The addition of Arteris NoC to the CoWare model library provides an unprecedented way to handle the vexing problems found in leading-edge SoCs," said A.K. Kalekos, vice president of marketing and business development for CoWare. "These problems include multiple IP and processors, clock domains, and wire and bus constraints. Now these problems can be solved within the best ESL design environment available today. We welcome Arteris as a supplier of critical, next-generation NoC technology."

Availability

Arteris NoC technology will be integrated into CoWare Platform Architect in the third quarter of 2006. The Arteris NoC Solution is available from Arteris now. Arteris and CoWare are working

together on the previously announced M4 project, headed by IMEC, for development of wireless multimedia SoCs for fourth generation cell phones. The joint solution will be demonstrated in the Arteris Booth #4263 at the 43rd Design Automation Conference in San Francisco. To see CoWare Platform Architect and other CoWare platform-driven ESL design solutions, visit CoWare's booth #3173 at the conference.

About Arteris

Arteris is the leading developer and solution provider of Network-on-Chip (NoC) IP, tools, and services. The Arteris solution is used by fabless semiconductor providers and integrated device manufacturers in applications where multiple SoCs are being integrated into a single design, process geometries are 90nm and smaller, and multiple processors and IP blocks are integrated into a single solution. The Arteris NoC IP and tools enable performance levels three times higher than bus-based alternatives at lower power, smaller die area and with much simpler development processes, enabling IP re-use and development cost savings. The Arteris NoC has been silicon proven by leading suppliers in the digital entertainment, wireless, and computing markets. Arteris is located in Guyancourt, France, a suburb of Paris. For additional information about Arteris, visit <http://www.arteris.com>.

About CoWare

CoWare is the leading supplier of platform-driven electronic system-level (ESL) design software and services. CoWare offers a comprehensive set of ESL tools that enable electronics companies to "differentiate by design" through the creation of system IP including embedded processors, on-chip buses, and DSP algorithms; the architecture of optimized SoC platforms; hardware/software co-design, and virtual platforms for software development. The company's solutions are based on open industry standards including SystemC. CoWare's customers are major systems, semiconductor, and IP companies in the market where consumer electronics, computing, and communications converge. CoWare's corporate investors include ARM [(LSE:ARM); (Nasdaq: ARMHY)], Cadence Design Systems (Nasdaq: CDNS), STMicroelectronics (NYSE: STM), and Sony Corporation (NYSE: SNE). CoWare is headquartered in San Jose, Calif., and has offices around the world. For more information about CoWare and its products and services, visit <http://www.coware.com>.

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