FlexNoC® Interconnect IP

Arteris IP FlexNoC network-on-chip (NoC) interconnect IP improves performance, development time, power consumption and die size of system on chip (SoC) devices for consumer electronics, mobile, automotive and other applications.

Benefits

SILICON PROVEN

FlexNoC is the first commercial NoC interconnect and is shipping in over 1.5 Billion chips. It is the backbone SoC interconnect used by Samsung, Mobileye, Altera (Intel), Hisilicon (Huawei) and other industry leaders for their most important projects.

STATE-OF-THE-ART TECHNOLOGY

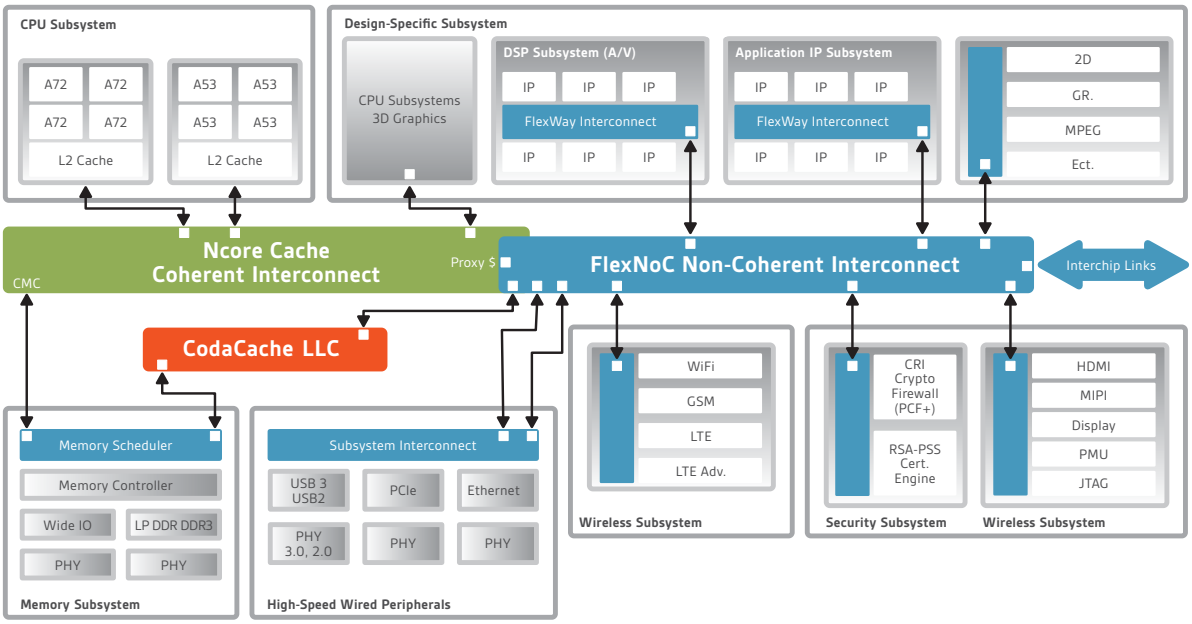
FlexNoC is continually updated with the latest technologies, including support for new protocols like AMBA® AHB5 and new capabilities like the FlexNoC Resilience Package for automotive ISO 26262 compliance and the PIANO Timing Assistance Package.

SCALABILITY & PRODUCTIVITY

Create SoCs using IP with any protocol (AMBA, OCP, PIF or proprietary) and scale up to 100s of IP blocks. Implement any topology (tree, ring, or mesh) while reducing development time through the use of automated simulation and verification technology.

Fast Facts

- Scales from 10s to 100s of IP blocks
- Protocol interoperability: AMBA AXI, AHB, APB; OCP; PIF; custom / proprietary
- Lowest die area & congestion
- Lowest latency & power
- Shortest design time
- Visual floorplan, area & timing closure estimation
- Integrated systemc simulation & UVM verification support
- Optimal QOS—bandwidth & latency
- Meet ISO 26262 ASIL D requirements



About Arteris IP

Arteris IP provides network-on-chip (NoC) interconnect IP and IP deployment technology to accelerate system-on-chip (SoC) semiconductor development and integration for a wide range of applications from AI to automobiles, mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Bosch, Baidu, Mobileye, Samsung, Toshiba and NXP. Arteris IP products include the Ncore® cache coherent and FlexNoC® non-coherent interconnect IP, the CodaCache® standalone last level cache, and optional Resilience Package (ISO 26262 functional safety), FlexNoC AI Package, and PIANO® automated timing closure capabilities. Customer results obtained by using Arteris IP products include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

Leading Industry Perspectives

"For years, Arteris IP technology has allowed us to continually increase the performance of each EyeQ ADAS SoC generation while reducing wire routing congestion and timing closure issues."

ELCHANAN RUSHINEK
VICE PRESIDENT OF ENGINEERING
MOBILEYE

"Arteris IP's FlexNoC interconnect allows us to more easily optimize and implement our chip architectures for ideal dataflow within our ADAS systems, ensuring processing elements avoid starvation and communications occur with minimum latency. We are happy to be working with the world leader in network-on-chip interconnect technology to develop our next generation of pioneering ADAS chips and systems."

DR. YU KAI
FOUNDER AND CEO
HORIZON ROBOTICS

"In our never-ending efforts to improve efficiency, we've found Arteris The Arteris FlexNoC interconnect IP helps us greatly by enabling not only high bandwidth on-chip communications but also load-balanced data traffic to off-chip memory, all while simplifying our backend timing closure."

JIAN OUYANG
PRINCIPAL ARCHITECT
BAIDU

"We are able to more efficiently design large scale automotive chips because we are able to see early in the design process the layout impacts of our SoC and NoC architecture choices. This is especially important when using leading edge 5nm semiconductor process technologies."

KAICHI YAMASHITA
HEAD OF THE AUTOMOTIVE BUSINESS UNIT
SOCIONEXT

"Over many years, FlexNoC interconnect IP has helped us accelerate implementation of our digital TV chip designs on our latest semiconductor process nodes. This core interconnect technology is required to develop complex and highly optimized chips in a predictable, low-risk fashion."

JAEYOUL LEE
VICE PRESIDENT
SAMSUNG ELECTRONICS

"The Arteris IP FlexNoC interconnect is much more efficient than competitive technologies. The state-of-the-art interconnect IP reduces the die area and power consumption of our unique architecture, which helps us to meet the market requirements."

ORR DANON
CEO
HAILO

ARTERIS IP®

595 Millich Drive, Suite 200
Campbell, CA, 95008
arteris-support@arteris.com
+1 408 470 7300