# FlexNoC® 5 Physically Aware Interconnect IP

Arteris FlexNoC 5 network-on-chip (NoC) physically aware interconnect IP improves development time, performance, power consumption, and die size of system-on-chip (SoC) devices for mobile, automotive, consumer, enterprise, and other applications.

## Benefits

### SILICON PROVEN

FlexNoC is the first commercial NoC IP and has shipped in over 3 billion chips. It is the backbone of SoC interconnect used by Samsung, Mobileye, Intel, and other industry leaders for their most important projects.

### STATE-OF-THE-ART TECHNOLOGY

FlexNoC 5 slashes the time needed to close timing compared to manual pipeline insertion methodologies, reducing overall schedule risk. Interconnect timing can be closed to reduce the number of costly P&R runs to confirm timing, along with shrinking interconnect area by 10-15% compared to manual pipeline insertion. Built-in physical awareness enhances layout quality-of-results (QoR) and productivity after importing user-defined and production (LEF/DEF) floorplans, automatically configuring pipelines to meet timing closure, and separating FlexNoC interconnect IP modules at a physical level so they can be routed efficiently within the SoC. FlexNoC 5 also supports protocols such as AMBA 5® ACE-Lite, AHB, and AXI and capabilities like the FlexNoC Functional Safety and Reliability options.

### SCALABILITY & PRODUCTIVITY

Create SoCs with 100s of IP blocks. Implement any topology, for example, tree, ring, or mesh, while reducing development time using automated simulation and verification technologies. FlexNoC 5 also introduces new productivity gains with the ability to export and import configuration data between Arteris Magillem Connectivity tooling.

## Fast Facts

- Scales from 10s to 100s of IP blocks
- Built-in physical awareness for visualization of floor-plan and automatic timing closure assistance
- Protocol interoperability: AMBA 5 ACE-Lite, AXI, AHB, APB; OCP; PIF
- Lowest die area & congestion
- Lowest latency & power
- Optimal QoS—bandwidth & latency
- Shortest design time
- Integrated SystemC simulation & UVM verification support
- Magillem import and IP-XACT export
- Functional Safety (FuSa) option helps meet ISO 26262 ASIL B and D requirements against random hardware faults