ARTERIS IP

Datasheet

FlexNoC® 5 Physically Aware Interconnect IP

Overview

FlexNoC 5 from Arteris is an indispensable IP generator for efficient, high-performance network-on-chip (NoC) designs. It revolutionizes SoC design with its advanced physical awareness, optimizing interconnects, reducing development time, improving performance, lowering power consumption, and minimizing die size. It automates design and verification tasks, supports tailored topologies, and enhances system responsiveness.

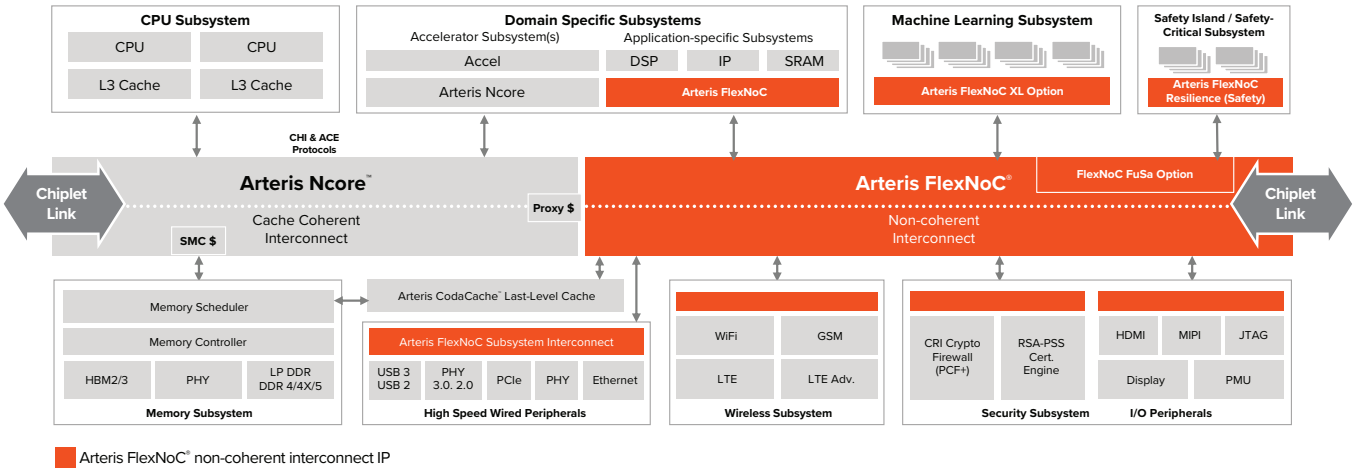
Physical awareness gives great visual design feedback early in the design cycle, accelerating timing closure, reducing area, and providing a great starting point for physical layout teams. In addition to the physically aware design flow, advanced power management, security, and QoS features extend battery life while maintaining system integrity and performance goals.

AMBA protocol support greatly eases IP integration tasks. At the same time, the FlexNoC FuSa Option provides functional safety support for designs targeting up to ASIL D.

FlexNoC 5 is the culmination of decades of development, resulting in a mature and proven solution trusted by industry leaders for secure, performant, and resilient designs in mobile, automotive, consumer, and enterprise applications.

Highlights

- Physically aware network-on-chip (NoC) for SoC development.
- Built-in physical awareness enhances layout quality and productivity.
- Reduces timing closure time and interconnect area compared to manual methods.
- Improves development time, die size, performance, and power consumption.
- Trusted by industry leaders like Samsung, Mobileye, Intel.
- Supports protocols: AMBA 5 ACE-Lite, AHB, AXI.
- Enables implementation of 100s of IP blocks with various topologies.
- Lowest die area, congestion, latency, and power consumption.
- Provides optimal QoS, integrated simulation, and verification support.
- FuSa Option helps to enable functional safety up to ASIL D.
- Magillem import/export for enhanced productivity.



Benefits

Improved development time.
FlexNoC 5 significantly reduces development time by streamlining the design process. It automates simulation and verification tasks, slashes timing closure time, and minimizes the number of costly iterations needed for confirming timing, thereby reducing overall schedule risks.

Enhanced performance.
With FlexNoC 5, SoCs achieve improved performance due to optimized interconnects. The product offers the flexibility to implement any topology, such as tree, ring, or mesh, allowing designers to tailor the interconnect structure to specific requirements. This, along with reduced latency and optimal Quality of Service (QoS) in terms of bandwidth and latency, contributes to overall performance gains.

Enhanced quality of results.
FlexNoC 5 incorporates built-in physical awareness, offering visualization of the floor plan and automatic timing closure assistance. It enhances the quality-of-results (QoR) and productivity by leveraging user-defined and production floorplans. The physical awareness feature also helps in separating FlexNoC interconnect IP modules at a physical level, facilitating efficient routing within the SoC and improving layout quality.

Reduced area cost.
FlexNoC 5 reduces the interconnect area by 10-15% compared to manual pipeline insertion methodologies. This die size optimization provides valuable space for integrating additional IP blocks or reducing overall chip size, contributing to cost savings and improved design efficiency.

Power consumption reduction.
FlexNoC 5 helps in minimizing power consumption in SoC designs. By optimizing the interconnect and providing advanced power management capabilities, it enables efficient power utilization, contributing to longer battery life and energy efficiency in mobile, automotive, and other power-constrained applications.

Flexible interoperability.
FlexNoC 5 supports industry-standard protocols such as AMBA 5 ACE-Lite, AHB, AXI, and others, ensuring seamless integration with various system designs. This protocol compatibility and interoperability simplify the integration of different IP blocks and peripherals within the SoC, enhancing flexibility and design scalability.

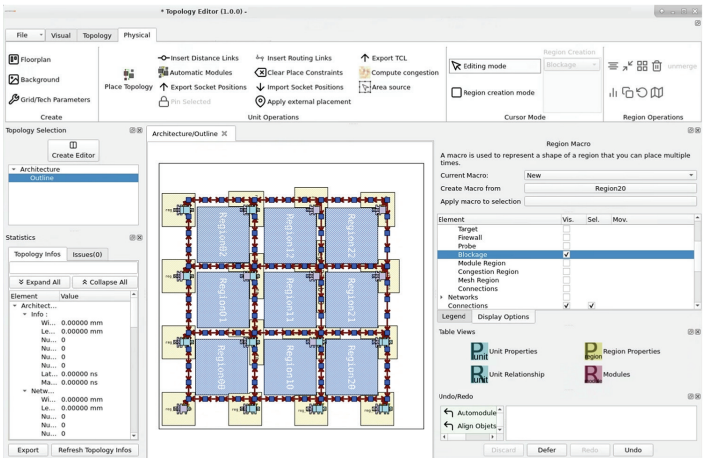
Functional safety and reliability.
FlexNoC 5 offers a Functional Safety (FuSa) option, which provides hardware-based data protection. This feature ensures increased reliability and functional safety of the SoC design, making it suitable for safety-critical applications. It helps SoC designs meet the requirements of functional safety standards such as ISO 26262 ASIL B and D against random hardware faults.

Scalability and productivity.
FlexNoC 5 enables the implementation of SoCs with hundreds of IP blocks. Its scalability allows for flexible design configurations and efficient utilization of available resources. Additionally, it introduces productivity gains through features like automated simulation and verification technologies, Magillem import/export support, and integrated SystemC simulation and UVM verification, which further streamline the design process.

Industry proven and trusted.
FlexNoC, as the first commercial NoC IP, has already shipped in over 3 billion chips. It is the backbone of SoC interconnect used by industry leaders such as Samsung, Mobileye, Intel, and others for their most important projects. The product's track record and widespread adoption demonstrate its reliability, performance, and value.

Features

NoC physical awareness.
FlexNoC 5 incorporates advanced physical awareness capabilities, allowing for visualization of the NoC's 2D mesh directly on the floorplan. This enables designers to have a clear understanding of the interconnect's physical implementation, optimizing layout quality and improving overall productivity.



Physically Aware Topology Editor GUI

Automatic timing closure assist.
FlexNoC 5 provides automatic timing closure assistance, streamlining the process of closing timing during design implementation. This feature reduces manual effort and accelerates the timing closure phase, minimizing design iterations and enhancing overall schedule predictability.

Network interfaces.
The product supports a wide range of network interfaces, including ACE-Lite, AXI, AHB, APB, OCP, and PIF. This comprehensive support ensures seamless integration with diverse IP blocks and peripherals, facilitating efficient communication and interoperability within the SoC.

AMBA 5 support, DVM v8.1.
FlexNoC 5 is fully compatible with the AMBA 5 specification, specifically supporting the DVM (Distributed Virtual Memory) version 8.1. This compatibility ensures compliance with the industry-standard AMBA protocol, enabling reliable and efficient data transfers within the SoC.

General transport capabilities.
FlexNoC 5 offers a versatile set of transport capabilities to accommodate various system requirements. It supports different topologies, including switches, FIFOs, converters, VC-Links, source-synchronous async bridges, broadcast/multicast, and reassembly buffer optimization. This flexibility enables designers to tailor the interconnect structure to meet specific design needs.

Quality of Service (QoS).
FlexNoC 5 provides advanced Quality of Service features, ensuring efficient bandwidth allocation and latency control within the interconnect. It incorporates a bandwidth regulator and limiter, allowing designers to define and enforce specific QoS requirements, guaranteeing optimal performance and resource utilization.

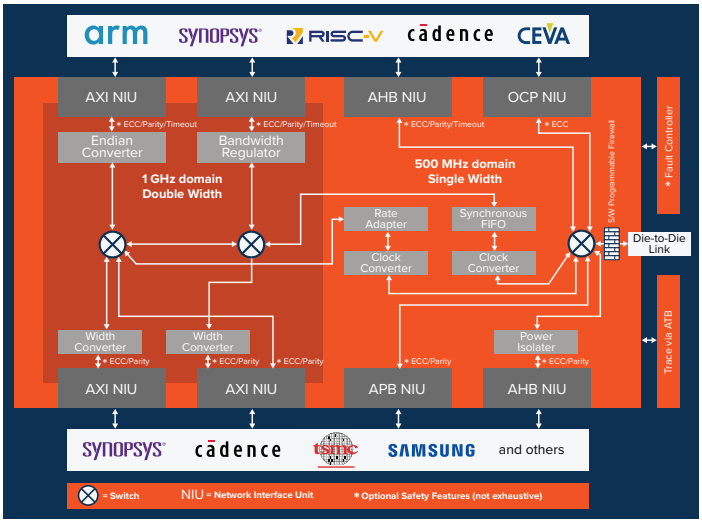
Domains.
The product supports multiple clock, power, and voltage domains, accommodating complex design requirements. FlexNoC 5 facilitates seamless integration of IP blocks operating at different clock frequencies or voltage levels, enabling efficient power management and domain-specific optimizations.

Power management.
FlexNoC 5 includes power management capabilities, including unit-level clock gating. This allows designers to selectively gate clocks to inactive units, minimizing power consumption and optimizing energy efficiency in the SoC design.

Security.
FlexNoC 5 offers native and user-defined firewall features, providing robust security mechanisms within the interconnect. This ensures secure data transfers and protects against unauthorized access or malicious attacks, enhancing the overall security of the SoC.

Safety – up to ISO 26262 ASIL D.
FlexNoC 5 supports safety-critical applications and complies with the ISO 26262 functional safety standard up to ASIL D level. This ensures that the interconnect reliably operates in safety-critical environments, providing the necessary level of safety and reliability required in automotive and other safety-critical applications.

In-silicon debug.
FlexNoC 5 incorporates in-silicon debug capabilities, enabling on-chip performance monitoring and debug functionalities. It supports the ATB (Advanced Trace Bus) 128b interface with timestamps, allowing for comprehensive and efficient debugging of the SoC's operation and performance.



FlexNoC 5 Example Configuration

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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