ARTERIS IP

Datasheet

FlexNoC® 5 & FlexWay™ 5 Functional Safety (FuSa) Option

Overview

Functional safety is a critical consideration in various industries, particularly in automotive and industrial applications, where the safety and integrity of systems are of utmost importance.

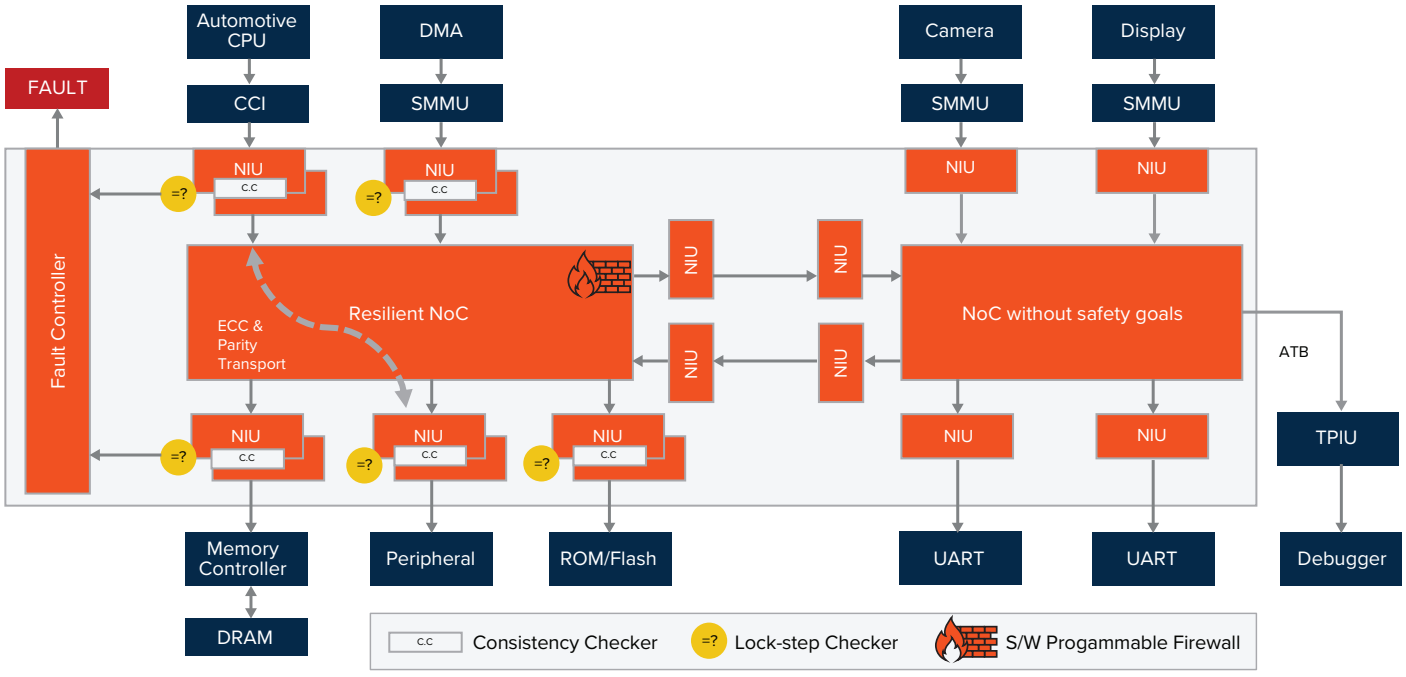
Choosing the Functional Safety Option of FlexNoC 5 or FlexWay 5 is an informed decision for those working in functional safety. It empowers designers to meet industry standards and regulations while providing the peace of mind that their systems adhere to the highest safety integrity levels.

CPU duplication and memory protection logic are no longer sufficient to address all the metrics required to meet the more stringent ISO 26262 ASIL and IEC 61508 SIL levels. Data traffic must now be protected throughout the chip floorplan.

Arteris provides a comprehensive set of functionality and documentation designed to address the stringent safety requirements of these industries. The Functional Safety Option is specifically tailored to help customers achieve up to ASIL D, the highest level of functional safety.

Highlights

- ISO 26262 ASIL D certifiable. Helps enable the highest level of functional safety.
- Comprehensive safety features. ECC, packet consistency checkers, unit duplication, initiator timeout, FMEDA generation, and fault reporting logic BIST.
- Error detection and correction. Ensure data integrity and system operation.
- Fault detection and redundancy. Enhance system reliability and resilience.
- Compliance with industry standards. Helps meet automotive and industrial safety requirements.
- Peace of mind. Helps to ensure end-user and environmental safety.



This functionality provides SoC designers with a solid foundation to build safety-critical systems. The option assists in creating a NoC IP capable of detecting and correcting errors, maintaining data integrity, and ensuring consistent and reliable operation. It also facilitates fault detection, redundancy, and error reporting, allowing the end system to promptly detect and respond to abnormal conditions.

Benefits

Enhanced safety compliance.
By incorporating these features into their design, SoC designers can aim to achieve the highest level of safety compliance, such as ASIL D, helping to ensure that their products meet strict industry standards.

Simplified safety implementation.
These features simplify the implementation of safety measures within the SoC design, saving designers valuable time and effort in developing and integrating the necessary safety mechanisms.

Increased reliability and resilience.
The functional safety option ensures data transmission and processing integrity and reliability by incorporating error detection and correction mechanisms. Including fault detection and redundancy, mechanisms enhance the overall system resilience, minimizing the impact of potential faults and failures. This results in a more robust and dependable SoC design.

Enhanced safety and security.
This is particularly critical in safety-critical applications, such as automotive and industrial environments, where the reliability and safety of the systems directly impact the well-being of individuals and the surrounding environment.

Reliable and fault-tolerant systems.
This ensures that the end-user experiences a reliable and resilient system that can detect and mitigate potential faults, thereby minimizing the risk of system failures or malfunctions.

Features

ECC at interface & in-transport.
Error correction code (ECC) is implemented at the interface and during data transport to detect and correct errors, ensuring data integrity and reliability.

Packet consistency checkers.
Packet consistency checkers verify the consistency of data packets during transmission, identifying any anomalies or errors that may occur.

Unit duplication - fault detection.
Units within the SoC design are duplicated to enable fault detection. This redundancy allows for detecting faults and the ability to fail in a known state.

Initiator timeout.
Initiator timeout functionality detects if an initiator fails to respond within a specified timeframe, triggering appropriate actions or safety measures to prevent system failures or hazards.

FMEDA generation.
Failure modes, effects, and diagnostic analysis (FMEDA) generation provides a comprehensive analysis of potential failure modes, their effects, and diagnostic capabilities. This analysis assists in identifying potential risks and implementing appropriate countermeasures.

Fault reporting logic BIST.
Built-in self-test (BIST) for fault reporting logic enables detecting and reporting of faults within the system, facilitating timely and accurate identification of any potential issues.

Complementary Product

FlexWay is a cost-efficient entry-level NoC product with an optimized feature subset of FlexNoC for smaller-scale SoC designs. Note that the FuSa Option is available to FlexWay and FlexNoC customers.

Both FlexNoC and FlexWay products can export IP-XACT files that can then be used in the Arteris Magillem import/export for enhanced productivity.

Other Arteris products with similar FuSa options are Ncore 3 cache-coherent NoC, and the CodaCache last-level/dedicated cache.

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

ARTERIS IP

arteris-support@arteris.com +1 408 470 7300

Copyright © 2004-2023 Arteris, Inc. All rights reserved worldwide. Arteris, Arteris IP, the Arteris IP logo and the other Arteris marks found at https://www.arteris.com/trademarks are trademarks or registered trademarks of Arteris, Inc. or its subsidiaries. All other trademarks are the property of their respective owners.

Rev 6/23