ARTERIS IP

Datasheet

FlexNoC® 5 Re-Order Buffer (ROB) Option

Overview

The Reorder Buffer (ROB) Option for FlexNoC 5 from Arteris is a critical innovation for enhancing memory performance in complex Network-on-Chip (NoC) systems. Tailored for high-throughput and efficiency applications, the ROB Option offers cutting-edge capabilities that drastically improve data flow management and memory interleaving across multiple channels.

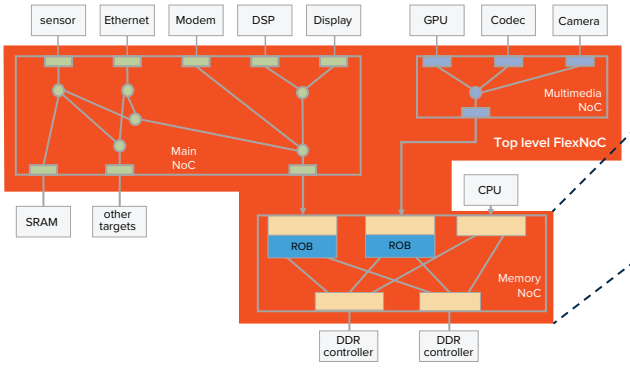
With the ROB Option, designers can seamlessly handle out-of-order memory responses, eliminating bottlenecks and maximizing memory channel utilization. By supporting concurrent reads across memory channels and enabling fine-tuned interleaving schemes, the ROB optimizes system performance without adding complexity to the initiators. This flexibility is particularly beneficial for systems with complex memory hierarchies or multiple memory controllers, such as advanced automotive, AI, and high-performance computing platforms.

In addition to improving latency and reducing response time, the ROB Option provides configurable buffer sizes and channel counts, allowing for tailored performance in both small and large-scale NoC designs. This makes the ROB Option an essential feature for FlexNoC 5, ensuring robust and scalable solutions that meet the demanding requirements of modern SoC architectures.

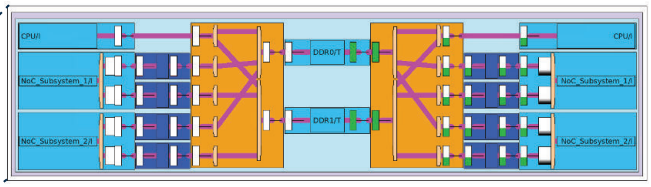
Highlights

- ROB prevents serialization bottlenecks and enables concurrent memory channel reads, improving overall system performance.
- Allows customization of buffer size and number of channels for different system requirements.
- Efficiently manages out-of-order responses, especially in systems with complex memory interleaving.
- Reduces latency and increases throughput by enabling out-of-order processing of multiple memory segments.
- Facilitates handling of complex interleaving schemes and non-contiguous address bit setups for memory controllers.

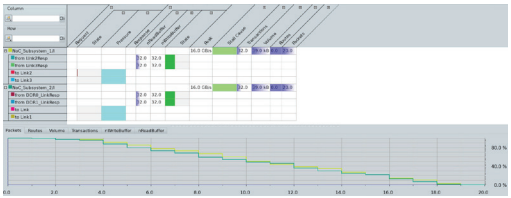
NoC Design



FlexNoC Design Environment



1. NoC Topology View



2. NoC Performance Exploration

Benefits

Eliminates bottlenecks.
Prevents response serialization bottlenecks, allowing for smoother and more efficient data flow.

Concurrent memory channel reads.
Enables simultaneous memory channel reads, improving overall throughput.

Handles out-of-order responses.
Efficiently manages out-of-order memory responses, ensuring correct data delivery and system performance.

Configurable.
Offers flexible configuration of buffer size and number of channels to optimize performance for specific system needs.

Supports complex interleaving.
Manages advanced memory interleaving schemes, allowing for improved memory access and utilization across multiple controllers.

Reduces latency.
Significantly decreases memory access latency, improving system responsiveness and efficiency.

Enhances scalability.
Facilitates system scalability by enabling better utilization of memory resources in both small and large NoC designs.

Improves resource utilization.
Maximizes memory controller efficiency by balancing data load and reducing congestion.

Features

Multi-Cycle SRAM and ECC support.
Enables enhanced memory integrity and error correction, ensuring reliable data transmission across channels.

Flip-flop or register file hard macros.
Offers flexibility in buffer implementation to optimize performance and design constraints.

Avoids network congestion.
Manages data across multiple channels to prevent congestion in the response network from separate memory targets.

Out-of-order capability for simple initiators.
Provides advanced out-of-order handling even for simple initiators, coalescing interleaved responses effectively.

Dynamic configuration in FlexNoC 5.
Easily configured within the FlexNoC 5 architecture for seamless integration during design and implementation phases.

Complementary Products

FlexWay is a cost-efficient entry-level NoC product with an optimized feature subset of FlexNoC for smaller-scale SoC designs and also supports the ROB option.

Both FlexNoC and FlexWay products can export IP-XACT files that can then be used in the Arteris Magillem import/export for enhanced productivity.

About Arteris

Arteris is a leading provider of system IP for the acceleration of system-on-chip (SoC) development across today's electronic systems. Arteris network-on-chip (NoC) interconnect IP and SoC integration technology enable higher product performance with lower power consumption and faster time to market, delivering better SoC economics so its customers can focus on dreaming up what comes next. Learn more at arteris.com.

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